INTERSIL
SYSTEMS DIVISION

ISB-3110
8085 Central Processor Card

FEATURES

- Full STD BUS Compatibility
- Fully Buffered Signals for System Expandability
- Up to 8K Bytes EPROM Capacity
- Up to 4K Bytes Static RAM Capacity
- Jumper Selectable (2716 or 2732 EPROMS)
- Full Memory Decoding Capability
- Full Bus Arbitration Circuitry
- Three Independent Timer/Counter Channels with Interrupting Capability
- Programmable Power-on Restart
- Power-on Reset and Pushbutton Reset Input
- 6.55 MHz Crystal Oscillator Frequency
- Internal/External Clock Selection
- Tri-state Address, Data and Control Bus
- Single +5V Supply

GENERAL DESCRIPTION

The ISB-3110 is a 8085 based STD BUS Microprocessor Card with 300ns clock time. The entire 8085-CPU Instruction Set can be used for programming without restriction. All signals to and from the STD BUS (address, data, and control) are fully tri-state buffered. Bus arbitration logic ensures proper arbitration between on-board vs. off-board memory, I/O, or interrupt acknowledge operations.

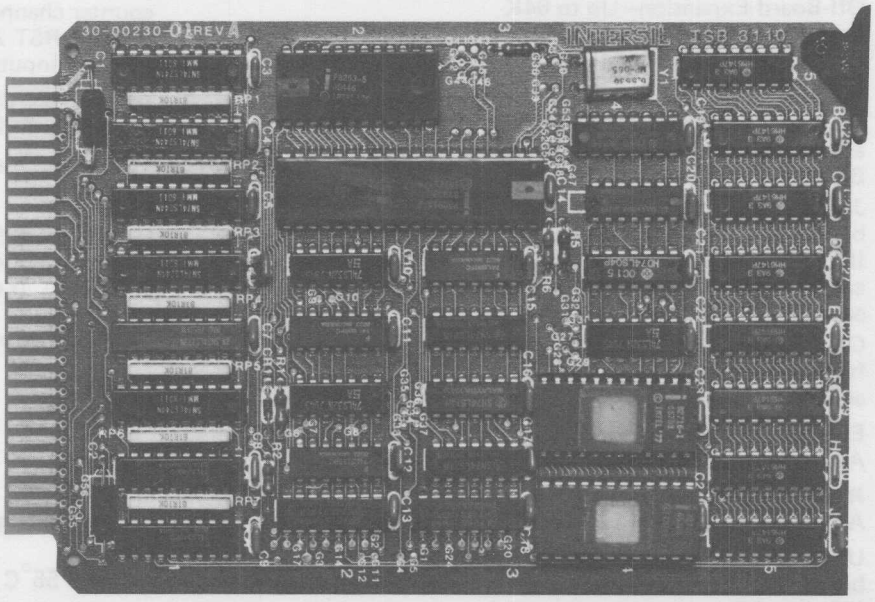
On-board static RAM memory in 1K Byte increments up to a maximum of 4K are provided. The popular 2114 (1K x 4) static RAM with 200ns access time is used. Two 24-pin sockets are provided for EPROM memory. Up to 4K Bytes of EPROM memory are available using 2716's (2K x 8) or up to 8K using 2732's (4K x 8).

Memory mapping for on-board RAMs and EPROMs is jumper selectable and can be mapped in 4K blocks anywhere in the 64K address field in 4K increments. The on-board RAMs and EPROMs can also be totally bypassed and removed from the card.

An on-board counter timer circuit provides three independent channels that provide counting and timing functions with interrupting capability and daisy chain priority arbitration. Timer counter interrupts utilize RST 7.5, 6.5 and 5.5 by connecting them to out 2, 1, or 0 of the timer counter.

Both on-board power-on reset and off-board pushbutton reset are implemented. The CPU on reset will start at 0000_H or can be programmed to jump to any location within the address field. If the latter is chosen, 3 bytes of the first EPROM on the board are used to store the jump address. After reading the starting address, the circuitry disables the EPROM or maps it at other preassigned locations other than 0000_H.

Jumper options include: CPU clock (internal/external), timer counter clock by channel (internal/external), on-board RAM starting address (anywhere in the 64K address field in 4K increments), on-board EPROM starting address (anywhere in the 64K address field in 4K increments), reset restart address (anywhere within on-board memory address range), EPROM selection (2716 or 2732).



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ISB-3110

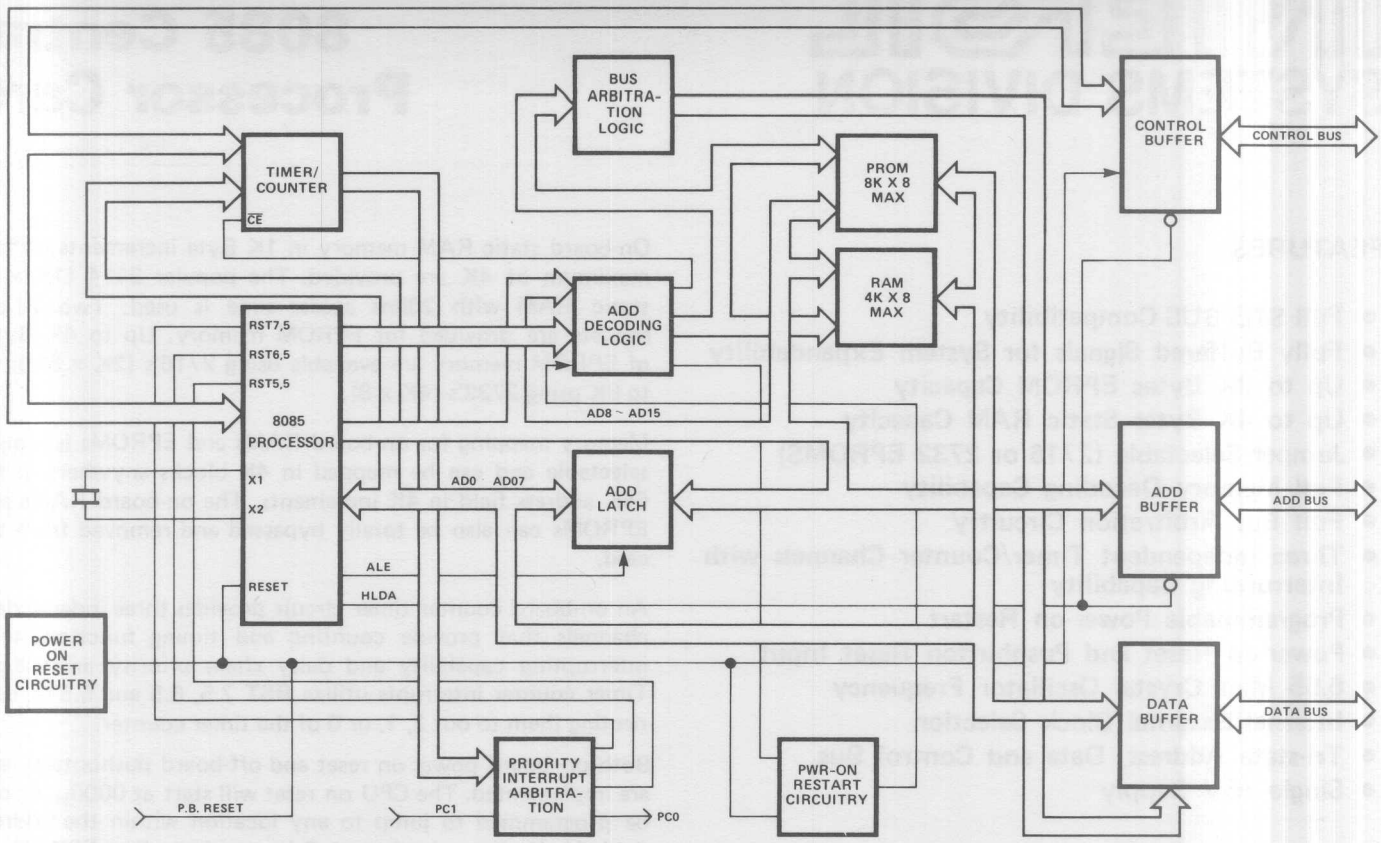


FIGURE 1. ISB-3110 Block Diagram

SPECIFICATIONS

Word Size:	8-Bit Data Bus Instruction: 8, 16, 24 Bits
Clock Period (T State):	300ns
Memory Capacity:	On-Board EPROMs—Up to 8K Bytes On-Board RAMs—Up to 4K Bytes Off-Board Expansion—Up to 64K Bytes, with Customer Specified Combination of RAMs, ROMs, EPROMs.
Memory Mapping:	On-Board EPROMs: Jumper Selectable 2716 (2K Bytes) or 2732 (4K Bytes). Jumper selectable for any 4K boundary within 64K address field. If 2732 is used, two 4K EPROMs can be mapped independently from each other within 64K address field. On-Board RAMs: Jumper selectable for any 4K boundary within 64K address field.
Memory Speed:	EPROM: 2716 or 2732 Access time: 400ns max. RAM: Dynamic or Static Access time: 400ns max.
I/O Capacity:	Up to 256 Bytes can be decoded off-board. The three port addresses, (7C, 7D, 7E) are used for the on-board Timer/Counter and can not be used for any off-board peripherals.
I/O Addressing:	On-Board programmable Timer

PORT ADDRESS (HEX)	CHANNEL
7C	0
7D	1
7E	2

Interrupts:	Multi-level vector interrupt with interrupt request originating from customer specified I/O only. Timer/counter channels interrupt CPU through RST 7.5, RST 6.5, RST 5.5 inputs.
Interface:	All Address, Data and Command signals are TTL compatible.
Power Requirements:	+5 VDC ±5% at 1.5 amps max.
Mating Connector:	See Table 1
Card Dimensions:	Height: 6.5 inches (16.51 cm) Width: 4.48 inches (11.38 cm) Thickness: 0.44 inches (1.12 cm)

(See Figure 3 For More Details)

ENVIRONMENTAL REQUIREMENTS

Operating Temperature:	0° to 55°C
Storage Temperature:	−40° to 80°C
Relative Humidity:	0% to 90% without condensation

TABLE 1. ISB-3110 Compatible Mating Connectors

INTERFACE	NO. OF PAIRS/PINS	CENTERS	CONNECTOR TYPE	VENDOR	VENDOR PART NO.
STD BUS	28/56	0.125 in.	Solder Tail	Viking Winchester	VH28/ICNK5 2HW28 D0–111
STD BUS	28/56	0.125 in.	Wire Wrap	Viking Winchester	VH28/ICHD5 HW28 D0–111

TABLE 2. STD BUS Organization and Specifications (With Pin Definitions)

The STD BUS pinout is organized into five functional groups:

Logic Power Bus	Pins 1–6
Data Bus	Pins 7–14
Address Bus	Pins 15–30
Control Bus	Pins 31–52
Auxiliary Power Bus	Pins 53–56

COMPONENT SIDE				CIRCUIT SIDE			
PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
1	+5V	In	+5 Volts DC (Bussed)	2	+5V	In	+5 Volts DC (Bussed)
3	GND	In	Digital Ground (Bussed)	4	GND	In	Digital Ground (Bussed)
5	–5V	In	–5 Volts DC	6	–5V	In	–5 Volts DC
7	D3	In/Out	Low Order Data Bus	8	D7	In/Out	High Order Data Bus
9	D2	In/Out	Low Order Data Bus	10	D6	In/Out	High Order Data Bus
11	D1	In/Out	Low Order Data Bus	12	D5	In/Out	High Order Data Bus
13	D0	In/Out	Low Order Data Bus	14	D4	In/Out	High Order Data Bus
15	A7	Out	Low Order Address Bus	16	A15	Out	High Order Address Bus
17	A6	Out	Low Order Address Bus	18	A14	Out	High Order Address Bus
19	A5	Out	Low Order Address Bus	20	A13	Out	High Order Address Bus
21	A4	Out	Low Order Address Bus	22	A12	Out	High Order Address Bus
23	A3	Out	Low Order Address Bus	24	A11	Out	High Order Address Bus
25	A2	Out	Low Order Address Bus	26	A10	Out	High Order Address Bus
27	A1	Out	Low Order Address Bus	28	A9	Out	High Order Address Bus
29	A0	Out	Low Order Address Bus	30	A8	Out	High Order Address Bus
31	$\overline{WR}$	Out	Write to Memory or I/O	32	$\overline{RD}$	Out	Read to Memory or I/O
33	$\overline{IORQ}$	Out	I/O Address Select	34	$\overline{MEMRQ}$	Out	Memory Address Select
35	$\overline{IOEXP}$	In/Out	I/O Expansion	36	$\overline{MEMEX}$	In/Out	Memory Expansion
37	$\overline{REFRESH}$	Out	Refresh Timing	38	$\overline{MCSYNC}$	Out	CPU Machine Cycle Sync
39	$\overline{STATUS\ 1}$	Out	CPU Status	40	$\overline{STATUS\ 0}$	Out	CPU Status
41	$\overline{BUSAK}$	Out	Bus Acknowledge	42	$\overline{BUSRQ}$	In	Bus Request
43	$\overline{INTAK}$	Out	Interrupt Acknowledge	44	$\overline{INTRQ}$	In	Interrupt Request
45	$\overline{WAITRQ}$	In	Wait Request	46	$\overline{NMIRQ}$	In	Non-Maskable Interrupt
47	$\overline{SYSRESET}$	Out	System Reset	48	$\overline{PBRESET}$	In	Push Button Reset
49	$\overline{CLOCK}$	Out	Clock from Processor	50	$\overline{CNTRL}$	In	AUX Timing
51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
53	AUX GND	In	AUX Ground (Bussed)	54	AUX GND	In	AUX Ground (Bussed)
55	AUX+V	In	AUX Positive (+12 Volts DC)	56	AUX–V	In	AUX Negative (–12 Volts DC)

TABLE 3. ISB-3110 STD BUS Signal Functions

SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
+5V	1 & 2	*+5 Logic Voltage (V_{CC})* – Main logic voltage lines (+5 volts). Both pins are bussed together for current capacity.
GND	3 & 4	*Logic Ground* – Ground for logic power. Both pins are bussed together for current capacity.
–5V	5 & 6	*–5 Logic Voltage* – Both pins are bussed together for current capacity.
D0–D7	7–14	*Data Bus* – An 8-Bit bidirectional tri-state bus. (Bidirectional means signals may flow either into or out of any card on the Bus). Direction of data is normally controlled by the processor card via the Control Bus. The data direction is normally affected by such signals as Read ($\overline{RD}$), Write ($\overline{WR}$) and Interrupt Acknowledge ($\overline{INTAK}$). The Data Bus uses high-level active logic levels. All cards are required to release the bus to a high impedance state when not in use. The Processor card releases the data bus in response to Bus Request ($\overline{BUSRQ}$) input from an alternate system controller, as in DMA transfers.
A0–A15	15–30	*Address Bus* – A 16-bit tri-state high-level active bus. The address will originate at the processor card or a bus controlling device. The processor card releases the Address Bus in response to a Bus Request ($\overline{BUSRQ}$) input from an alternate controller. The Address Bus provides 16 address lines for decoding by either memory or I/O. Memory request ($\overline{MEMRQ}$) and I/O request ($\overline{IORQ}$) control lines are used to distinguish between the two operations.
$\overline{WR}$	31	*Write to Memory or I/O* – A tri-state, active-low control line that indicates the BUS holds valid data to be written in the addressed memory or output device.
$\overline{RD}$	32	*Read from Memory or I/O* – A tri-state, active-low control line that indicates the processor or other bus controlling device wants to read data from memory or an I/O device. The selected I/O device or memory should use this signal to gate data onto the BUS.
$\overline{IORQ}$	33	*I/O Address Select* – A tri-state, active-low processor output control line. $\overline{IORQ}$ indicates that the address lines hold a valid I/O address for an I/O Read or Write.
$\overline{MEMRQ}$	34	*Memory Address Select* – A tri-state, active-low memory request line. $\overline{MEMRQ}$ indicates that the Address Bus holds a valid address for memory read or memory write operations.
$\overline{IOEXP}$	35	*I/O Expansion* – An active-low control signal used to expand or enable I/O Port addressing.
$\overline{MEMEX}$	36	*Memory Expansion* – An active-low control signal used to expand or enable memory addressing.
$\overline{REFRESH}$	37	*Dynamic Memory Refresh* – a tri-state, active-low control line normally used to refresh dynamic memory. This signal is not generated on this processor card.
$\overline{MCSYNC}$	38	*Machine Cycle Sync* – A tri-state, active-low processor output signal that occurs once during each processor machine cycle. (Machine cycle is defined as the sequence that involves Addressing, Data Transfer and Execution.) $\overline{MCSYNC}$ defines the beginning of the machine cycle.
$\overline{STATUS\ 1}$	39	*Status Control Line 1* – Used in conjunction with $\overline{STATUS\ 0}$ to indicate the type of CPU cycle in progress.

TABLE 3. ISB-3110 STD BUS Signal Functions (Continued)

SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
$\overline{\text{STATUS 0}}$	40	*Status Control Line 0* – Used in conjunction with $\overline{\text{STATUS 1}}$ to indicate the type of CPU cycle in progress.
$\overline{\text{BUSAK}}$	41	*BUS Acknowledge* – An active-low output line. The processor responds to a $\overline{\text{BUSRQ}}$ by releasing the BUS and giving an Acknowledge signal on the $\overline{\text{BUSAK}}$ line. $\overline{\text{BUSAK}}$ occurs at the completion of the current machine cycle.
$\overline{\text{BUSRQ}}$	42	*Bus Request* – An active-low input line. A $\overline{\text{BUSRQ}}$ causes the processor to suspend operations on the BUS by releasing all tri-state BUS lines for use by another processor. The BUS is released once the current machine cycle is completed.
$\overline{\text{INTAK}}$	43	*Interrupt Acknowledge* – An active-low output line from the processor card that occurs in response to ($\overline{\text{INTRQ}}$). It is used to tell the interrupting device that the processor card is ready to respond to the Interrupt. For vectored interrupts the vector address is placed on the Data Bus by the interrupting device during $\overline{\text{INTAK}}$.
$\overline{\text{INTRQ}}$	44	*Interrupt Request* – An active-low processor card input line that conditionally interrupts the program. It is masked and ignored by the processor unless deliberately enabled by a program instruction. If the processor accepts the interrupt, it acknowledges by dropping $\overline{\text{INTAK}}$.
$\overline{\text{WAITRQ}}$	45	*Wait Request* – An active-low input line to the processor that suspends processor operations as long as it remains low. The processor will hold in a state that maintains a Valid Address on the Address Bus.
$\overline{\text{NMIRQ}}$	46	*Non-Maskable Interrupt* – An active-low processor card interrupt input line of highest priority.
$\overline{\text{SYSRESET}}$	47	*System Reset* – An active-low output from the system reset circuit. The system reset circuit is triggered by power-on detection or by the pushbutton reset. The system reset bus line should be applied to all cards on the BUS that have latch circuits requiring initialization.
$\overline{\text{PBRESET}}$	48	*Push Button Reset* – An active-low input line to the processor.
$\overline{\text{CLOCK}}$	49	*Clock From Processor* – A buffered processor clock signal used for system synchronization or as a general clock source.
$\overline{\text{CNTRL}}$	50	*Control* – An external clock input for special clock timing.
PCO	51	*Priority Chain Output (Output, active-high)* – This signal is sent to the PCI input of the next lower card in the priority chain. A card that needs priority should hold PCO low.
PCI	52	*Priority Chain In (Input, active-high)* – This signal is provided directly from the PCO of the next higher card in the priority chain. A high level on PCI gives priority to the card sensing the PCI input.
AUX GND	53 & 54	*Auxiliary Ground* – Ground for AUX Power. Both pins bussed together for current capacity.
AUX +V	55	*Auxiliary Positive Voltage (+12 Volts DC)*
AUX –V	56	*Auxiliary Negative Voltage (–12 Volts DC)*

TABLE 4. ISB-3110 AC Characteristics

SYMBOL	PARAMETER	8085A-2[2] (PRELIM) MIN (ns)	8085A-2[2] (PRELIM) MAX (ns)
t_{CYC}	$\overline{CLK}$ Cycle Period	200	2000
t_1	$\overline{CLK}$ Low Time	40	
t_2	$\overline{CLK}$ High Time	70	
t_r, t_f	$\overline{CLK}$ Rise and Fall Time		30
t_{AC}	A_{8-15} Valid to Leading Edge of Control[1]	115	
t_{ACL}	A_{0-7} Valid to Leading Edge of Control	115	
t_{AD}	A_{0-15} Valid to Valid Data In		350
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0
t_{AL}	A_{8-15} Valid Before Trailing Edge of $\overline{SYNC}$[2]	50	
t_{ALL}	A_{0-7} Valid Before Trailing Edge of $\overline{SYNC}$	50	
t_{ARY}	$\overline{WAIT}$ Valid from Address Valid		100
t_{CA}	Address (A_{8-15}) Valid After Control	60	
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) Edge of $\overline{SYNC}$	230	
t_{CL}	Trailing Edge of Control of $\overline{SYNC}$	25	
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	230	
t_{HABE}	$\overline{BUSAK}$ to Bus Enable		150
t_{HABF}	Bus Float After $\overline{BUSAK}$		150
t_{HACK}	$\overline{BUSAK}$ Valid to Trailing Edge of $\overline{CLK}$	40	
t_{HDH}	$\overline{BUSRQ}$ Hold Time	0	
t_{HDS}	$\overline{BUSRQ}$ Setup Time to Trailing Edge of $\overline{CLK}$	120	
t_{INH}	$\overline{INTR}$ Hold Time	0	
t_{INS}	$\overline{INTR}$, Setup Time to Falling Edge of $\overline{CLK}$	150	
t_{LA}	Address Hold Time After $\overline{SYNC}$	50	
t_{LC}	Trailing Edge of $\overline{SYNC}$ to Leading Edge of Control	60	
t_{LCK}	$\overline{SYNC}$ High During $\overline{CLK}$ Low	50	
t_{LDR}	$\overline{SYNC}$ to Valid Data During Read		270
t_{LDW}	$\overline{SYNC}$ to Valid Data During Write		120
t_{LL}	$\overline{SYNC}$ Width	80	
t_{LRY}	$\overline{SYNC}$ to READY Stable		30
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	90	
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		150
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	220	
t_{RDH}	Data Hold Time After $\overline{READ}$ $\overline{INTA}$	0	
t_{RYH}	$\overline{WAIT}$ Hold Time	0	
t_{RHS}	WAIT Setup Time to Leading Edge of $\overline{CLK}$	100	
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	60	
t_{WDL}	LEADING Edge of $\overline{WRITE}$ to Data Valid		20

Notes:

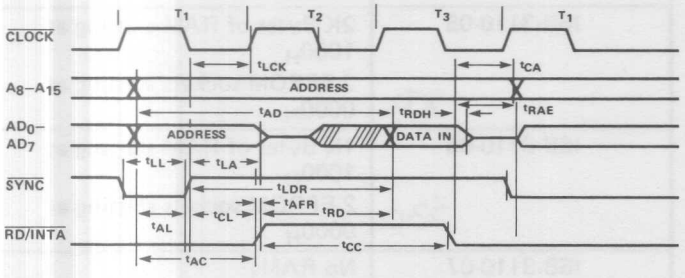
1. A_8–A_{15} address Specs apply to IO/M, S_0, and S_1 except A_8–A_{15} are undefined during T_4–T_6 of OF cycle whereas $\overline{MREQ}$, $\overline{IORQ}$ and S_1 are stable.
2. Test conditions: t_{CYC} = 320ns (8085A)/200ns (8085A-2); C_L = 150pF.
3. For all output timing where C_L = 150pF use the following correction factors:
   25pF ≤ C_L < 150pF: −0.10ns/pF
   150pF < C_L ≤ 300pF: +0.30ns/pF
4. Output timings are measured with purely capacitive load.
5. All timings are measured at output voltage V_L = 0.8V, V_H = 2.0V, and 1.5V with 20ns rise and fall time on inputs.
6. To calculate timing specifications at other values of t_{CYC}, use Table 5.

TABLE 5. ISB-3110 Timing Equations

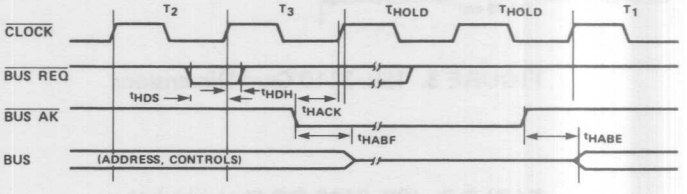
SYMBOL	EQUATIONS	LIMIT
t_{AL}	(1/2) T – 50	Min.
t_{LA}	(1/2)T – 50	Min.
t_{LL}	(1/2) T – 20	Min.
t_{LCK}	(1/2) T – 50	Min.
t_{LC}	(1/2) T – 40	Min.
t_{AD}	(5/2 + N) T – 150	Max.
t_{RD}	(3/2 + N) T – 150	Max.
t_{RAE}	(1/2) T – 10	Min.
t_{CA}	(1/2) T – 40	Min.
t_{DW}	(3/2 + N) T – 70	Min.
t_{WD}	(1/2) T – 40	Min.

SYMBOL	EQUATIONS	LIMIT
t_{CC}	(3/2 + N) T – 70	Min.
t_{CL}	(1/2) T – 75	Min.
t_{ARY}	(3/2) T – 200	Max.
t_{HACK}	(1/2) T – 60	Min.
t_{HABF}	(1/2) T + 50	Max.
t_{HABE}	(1/2) T + 50	Max.
t_{AC}	(2/2) T – 85	Min.
t_1	(1/2) T – 60	Min.
t_2	(1/2) T – 30	Min.
t_{RV}	(3/2) T – 80	Min.
t_{LDR}	(4/2) T – 30	Max.

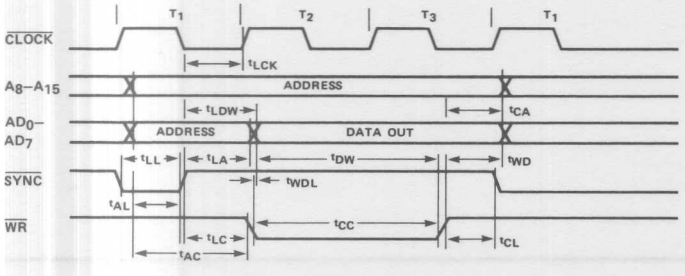
NOTE: N is equal to the total WAIT states. $T = t_{CYC}$.



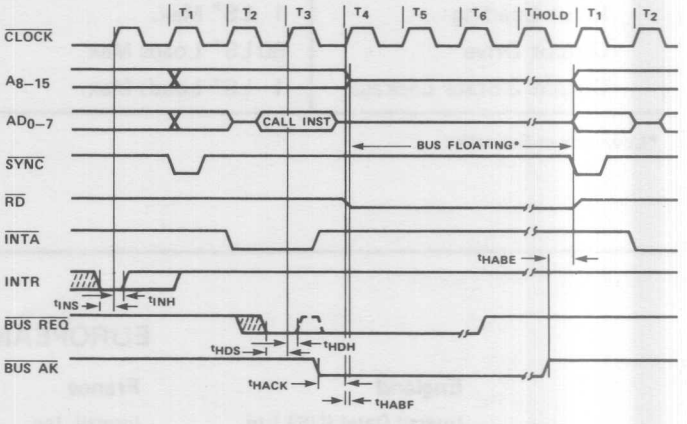
READ OPERATION



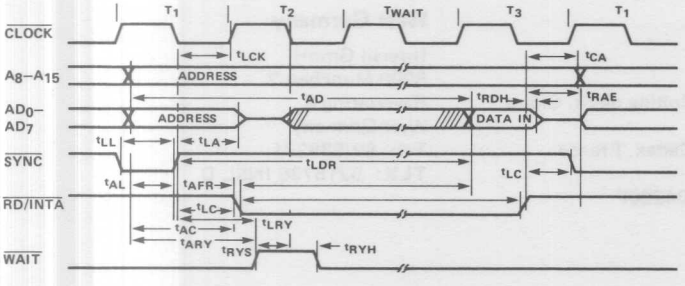
BUS REQUEST OPERATION



WRITE OPERATION



INTERRUPT AND BUS REQUEST



READ operation with WAIT CYCLE (Typical)
(same READY timing applies to WRITE operation)

FIGURE 2. ISB-3110 Timing Diagrams

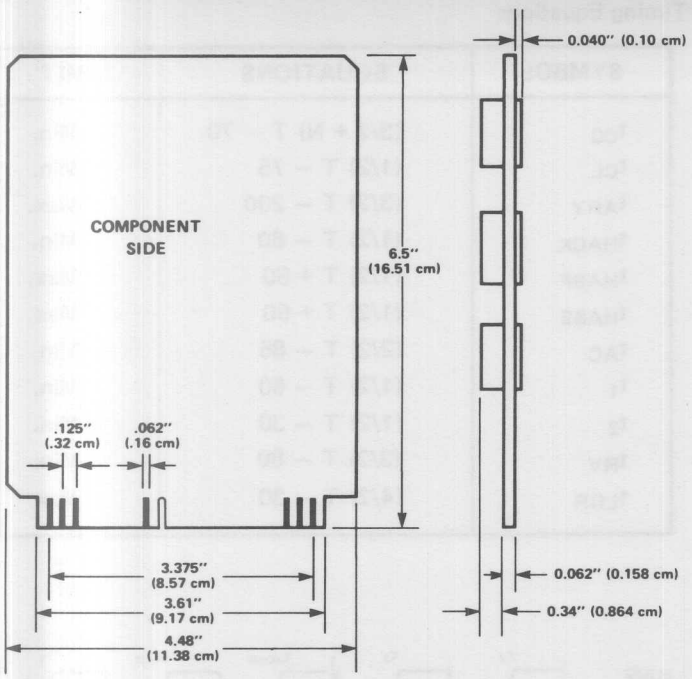


FIGURE 3. ISB-3110 Card Dimensions

TABLE 6. ISB-3110 DC Characteristics

PARAMETER	LIMITS
Power V_{CC}	5V ±5% at 1.5A Max.
Operating Temperature	0 to 55°C
Input Loading	1 LS* Max.
Output Drive	60 LS* Loads Max.
Output 3-State Leakage	1 LS* Loads Max.

*Low-power Schottky

ORDERING INFORMATION

ORDERING PART NO.	DESCRIPTION
ISB-3110-01	4K Bytes of RAM strapped to start at 1000_H Two EPROM sockets strapped to start at 0000_H
ISB-3110-02	No internal RAM, one EPROM supplied with first 3 bytes programmed to power-on start the CPU at location $E000_H$
ISB-3110-03	One EPROM with first 3 Bytes programmed to power-on start the CPU at $E000_H$. 2K bytes of RAM mapped at $E800_H$.
ISB-3110-04	3K Bytes of RAM starting at 1000_H 2 EPROM sockets starting at 0000_H
ISB-3110-05	2K Bytes of RAM starting at 1000_H 2 EPROM sockets starting at 0000_H
ISB-3110-06	1K Bytes of RAM starting at 1000_H 2 EPROM sockets starting at 0000_H
ISB-3110-07	No RAMs 2 EPROM sockets starting at 0000_H

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